Power switching device

Improvement of switching loss by driver source

Power switching devices such as MOSFETs and IGBTs are used as switching elements in various applications and power grid. Switching and conduction losses of the power devices need to be reduced as much as possible, to increase the efficiency of the system. Several approaches can be implemented to reduce the losses. In recent years, package technology equipped with driver source terminal (also called Driver source or Kelvin source) is one of these approaches. This application note shows the influence of the driver source terminal on the switching behavior. Moreover, the usage precautions are also described.

Switching behavior of MOSFETs

MOSFETs are voltage-driven switching devices. The switching operation of MOSFET can be controlled by turning on and off the voltage applied to the gate terminal. Figure 1 shows example of gate driving circuit for a MOSFET with conventional TO-247 package (as called TO-247N).
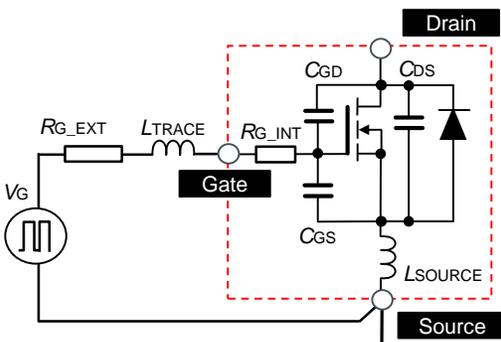

Figure 1. Example of conventional gate driving circuit for MOSFET

It is very important to take care of following parameters for switching the power device. The switching speed can be controlled by an external resistor R_{G_EXT} between the drive power source V_G and the gate terminal (Gate). The switching behavior is also influenced by the stray inductance L_{TRACE} presents on the gate path, due to the PCB layout, and by the source stray inductance L_{SOURCE} present on the source terminal of MOSFET, due to the package. The package inductance of the gate terminal is included in L_{TRACE}, and the inductance L_{DRAIN} of the drain terminal is not included in the gate drive

circuit because is not needed for this analysis.

The general operation of a drive circuit has been vastly described in the literature and the details will not be explained and described in this application note. However, the influence of L_{SOURCE} on the switching behavior is easily overlooked at the conventional switching behavior analysis. There is a voltage drop $V_{LSOURCE}$ across L_{SOURCE}, which depend on the change of the drain current I_D flowing between the drain and source over time ($V_{LSOURCE} = L_{SOURCE} \cdot dI_D/dt$).

Figure 2 shows the voltage transitions during switching operation of the drive circuit. When V_G rises, the MOSFET turns on, I_D increases and it generates a voltage drop $V_{LSOURCE}$ across L_{SOURCE} towards direction (I), as indicated in the figure. On the other hand, since current I_G flows into the gate, voltage drops V_{RG_EXT} (I) across R_{G_EXT}. The internal gate-source voltage V_{GS_INT} is influenced by the stray inductance and R_{G_EXT} according to (1), the influence of L_{TRACE} has been neglected due the it small value

$$V_{GS\_INT} = V_G - I_G * R_{G\_EXT} - L_{SOURCE} * \frac{dI_D}{dt} \qquad (1)$$

During the turn-on transient, V_{GS_INT} decreases (I_G and dI_D/dt are positive), and as result the switching speed also decreases, and therefore, the turn-on losses are increased.

During the turn-off transient, V_{GS_INT} increases, because I_G and dI_D/dt become negative, the voltage drop across R_{G_EXT} and L_{SOURCE} are as indicated by (II) in the Figure. As a result, turn-off speed decreases, and therefore, the turn-off losses are increased.

L_{SOURCE} of power switching device generally is a several nH to dozen of nH. A feature of SiC MOSFETs is the fast switching, the dI_D/dt can be in the range of A/ns, which can lead in a voltage drop $V_{LSOURCE}$ above 10 V. As a consequence, the switching behavior is highly influenced.
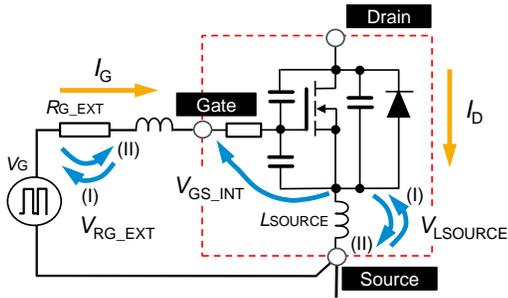

Figure 2. Voltage transition during switching operation of MOSFET

To overcome this problem, the driver source terminal has been introduced, which improves the switching speed by eliminating the influence of $V_{LSOURCE}$.

Package with Driver Source terminal

Figure 3 shows an example of two packages with driver source terminal and the pin assignments. ROHM has introduced in the market the (a) TO-247-4L and the (b) TO-263-7L packages.
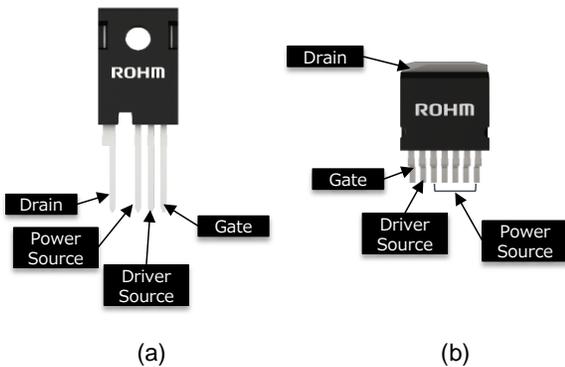

Figure 3. Package with driver source terminal
(a) TO-247-4L, (b) TO-263-7L

Effectiveness by driver source terminal

Figure 4 shows the drive circuit of a MOSFET with driver

source terminal. The only difference from the conventional drive circuit (Figure 2) is that the gate drive is connected to the driver source terminal of MOSFET instead to the power source.
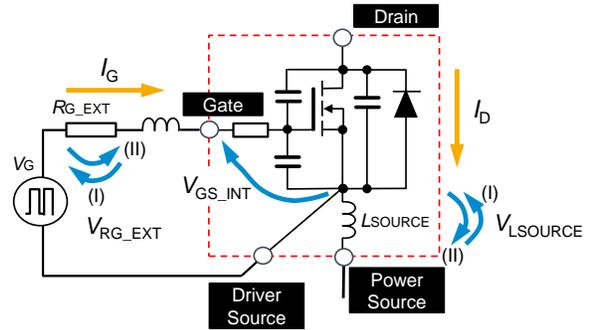

Figure 4. Example of Gate drive circuit for MOSFET with driver source terminal

As shown in figure.4, switching behavior is no longer influenced by $V_{LSOURCE}$, because L_{SOURCE} is no longer common to the gate drive loop. V_{GS_INT} voltage is represented by (2).

$$V_{GS\_INT} = V_G - I_G * R_{G\_EXT} \qquad (2)$$

Comparison by double pulse test

In order to compare the switching behavior of power devices between packages with driver source terminal and conventional package (without driver source), a double pulse test has been performed using the low side (LS) switch MOSFET (Figure 5). The gate of the high side (HS) MOSFET is connected to source terminal (in case of 3 pin packages) or driver source terminal trough R_{G_EXT}. Only its body diode is used for the commutation.
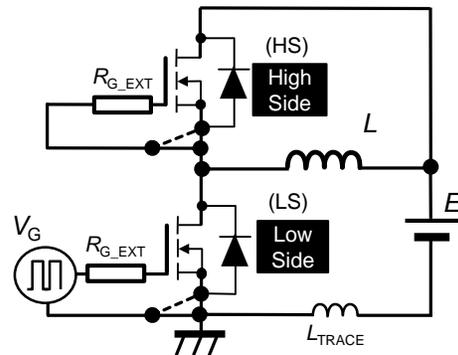

Figure 5. Circuit of double pulse switching test

The test conditions are:

- $R_{G\_EXT} = 10\Omega$,
- $V_{HVDC} = 800V$ (Voltage supply), and
- $I_D = 50A$.

The MOSFETs used in the test are 1200 V devices with an on-resistance (RDS (on)) of 40mΩ in different packages:

1. a conventional TO-247N 3 pin package (SCT3040KL),
2. a 4 pin package TO-247-4L (SCT3040KR) with driver sources terminal, and
3. a 7 pin package TO-263-7L (SCT3040KW7) also with driver source terminal.

Figure 6 shows the waveforms during the turn-on transient of the drain-source voltage V_{DS}, drain current I_D (Figure 6a) and the switching losses (Figure 6b). The turn-off transient is shown in Figure 7.

During the turn-on process (Figure 6), the drain current I_D of the power device with the driver source terminal rises sharply compared to the device with a conventional package. With the kelvin source packages the drain-source voltage at turn-on is dropping much faster, as the device remains at the miller plateau much shorter since the effective gate-voltage is higher. As a result, the switching loss is reduced by 24% in case of 7 pin package and by 38% in case of 4 pin package.

However, the I_D peak of TO-247-4L package is 23A larger than the peak with the TO-247N package. This is because the charge and discharge time of C_{OSS} is reduced by the high speed switching, due to the effectiveness of the driver source.

The energy to charge and discharge C_{oss} is constant (V_{HVDC} constant to 800V), therefore a faster switching increases the peak value of this charge current. This current peak is not due to self-turn-on behavior of the HS MOSFET. However, if drive circuit for packages of TO-247-4L and TO-263-7L has no countermeasure to avoid self-turn on behavior, the peak current during turn-on may increase.

In addition, I_D peak of TO-263-7L is 60A and it is not in the same range of peak current of TO-247-4L. It is due to the differences of the package inductance of the MOSFETs. During the turn on transient, V_{DS} of the low side MOSFET decreases due to dI_D/dt and the stray inductance in the commutation loop. As consequence, the C_{OSS} is partially discharged. In case of the TO-263-7L, V_{DS} drops less than the TO-247-4L, due to the

lower stray inductance, and therefore, the discharge current for the TO-247-4L decreases, and as a consequence the I_D peak decreases too. For the same reason, the turn on loss E_{ON} with the TO-247-4L package are lower.

It is recommended to implement countermeasures as miller clamping circuit, and/or a capacitor in the range of nF between gate and source. Please for further information regarding this topic, refers to the application note "Surge suppression of gate-source voltage" (*2).
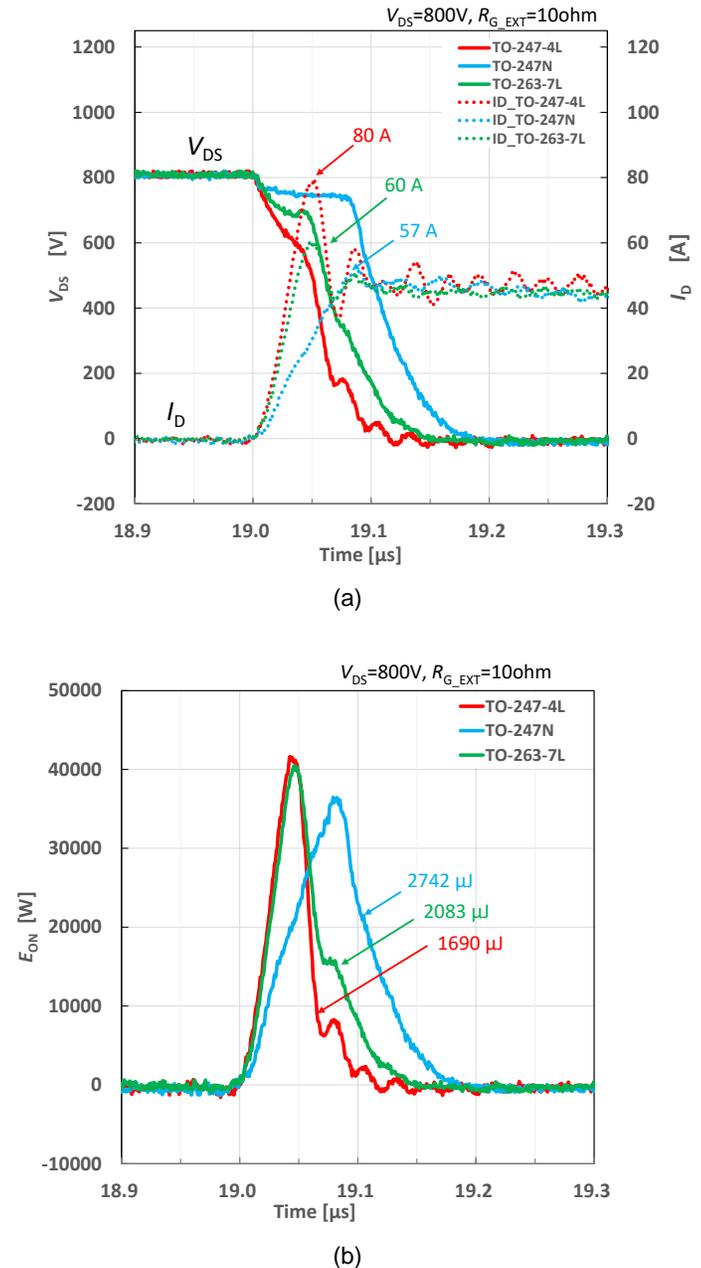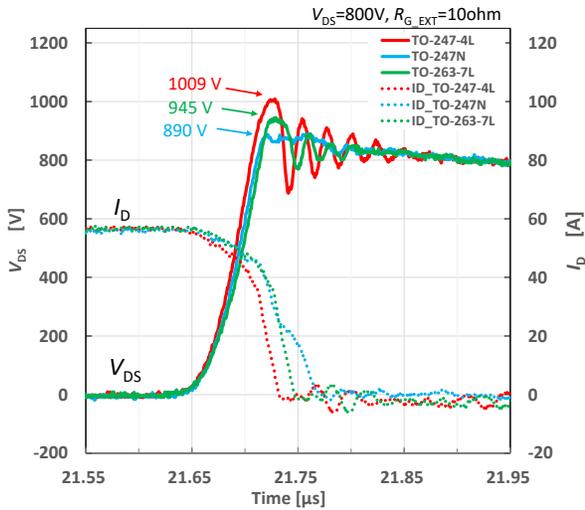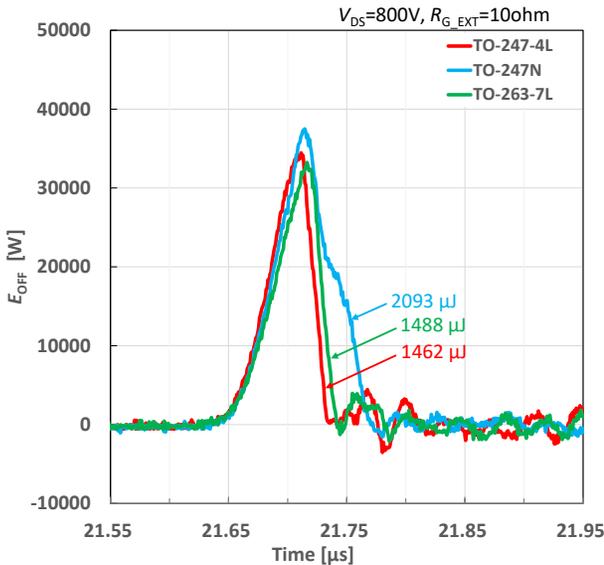

(a)

(b)

Figure 6. Waveform Turn-on

(a) V_{DS}, I_D, (b) Switching loss

The turn-off behavior of packages with driver source terminal shows an improvement by 30% (Figure 7).

V_{DS}=800V, R_{G_EXT}=10ohm

(a)

V_{DS}=800V, R_{G_EXT}=10ohm

(b)

Figure 7. Waveform Turn-off
(a) V_{DS}, I_D, (b) Switching loss

The turn-off surge voltage observed in the waveform of V_{DS} during turn-off is caused by the total parasitic inductance in the main circuit L_{TRACE}, in this case 2*(L_{DRAIN} + L_{SOURCE}) as shown in Figure 5 (other stray inductances e.g. due to layout are neglected). For this reason, the surge voltage increases with increasing dI_D/dt. The surge voltage in case of TO-247-4L

package is about 119V larger than the overvoltage with TO-247N package. Countermeasures for suppressing surge voltage such as snubber circuits may be required.

The TO-263-7L has overall small package inductance, therefore the surge voltage is smaller compared to the one with the TO-247-4L package. The smaller the total stray inductance of the power current path is, the smaller the surge voltage is.

Table 1 summarizes the switching losses of each package.

Table 1. Comparison of Eon, Eoff
V_{DS}=800V, I_D=50A, R_{G_EXT}=10Ω

DUT	Eon [µJ]	Eoff [µJ]
SCT3040KL	2742	2093
SCT3040KR	1690	1462
SCT3040KW7	2083	1488

Behavior of Gate-Source signal at Bridge configuration

One of the most common configurations in power switching topology is the bridge configuration, as shown in Figure 5. However as described in the application note "Behavior of gate-source voltage in bridge configuration" (*1), the switching behavior of TO-247-4L and TO-263-7L is different from case of TO-247N. It is quite important to recognize details in order to implement the countermeasures for the gate-source surge voltages.

Figure 8 and Figure 10 show the switching waveforms of TO-247-4L in bridge configuration and the LS power device switch. Figure 8 shows turn-on, and Figure 10 shows turn-off transient.

At first, this application note explains behavior during turn-on focused mainly differences with TO-247N. Please refer for more details about the turn-off operation of the TO-247N to the "gate in the bridge configuration behavior of the source voltage"(* 1).

The horizontal axis of Figure 8(a) and Figure 10(a) represents time. The definition of time domain Tk (with k =1…8) is as follows shown in (I) to (VII). Event (III) occurs immediately after the end of period T2, and event (VII) occurs immediately after the end of period T5.

T1: LS is turning ON and current is changing（Event (I)）

T2: LS is turning ON and voltage is changing（Event (II)）

T3: LS stays ON status

T4: LS is turning OFF and voltage changing（Event (IV)）

T5: LS is turning OFF and current changing（Event (VI)）

T4-T6: Dead-time, until HS is turned ON

T7: HS stays ON　（Synchronous rectification）

T8: Dead-time until HS is turned OFF and LS is turned ON

(a)

Only the event (I) of TO-247-4L is significantly different from case of TO-247N, and observes a V_{GS} positive surge on the commutation side (HS), in case of TO-247N it was negative surge voltage. This is caused by the current I_{CGD} shown in (I) in Figure 8(b), which shows the behavior of the current at the gate path. This current is flowing through C_{GD}.

Before the switching transient, the commutation current I_{D_HS} flows from source to drain through body diode of HS MOSFET, when switching transient starts, I_{D_LS} increases and I_{D_HS} decreases. On the other hand, forward voltage V_{F_HS} of SiC MOSFET's body diode (circled by the dotted line in Figure 8 (a)) is generally more current-dependent than that of Si MOSFET, so dI_{D_HS}/dt and dV_{F_HS}/dt gets larger according to acceleration of switching speed. The positive dV_{DS_HS}/dt of the HS MOSFET leads into current I_{CGD} flowing through C_{GD} from Drain to Gate path, and as consequence the gate-source voltage increases. In the conventional TO-247N, the current change of I_{D_LS} is small, and it is expected that the I_{CGD} as event (I) might be hardly observed.
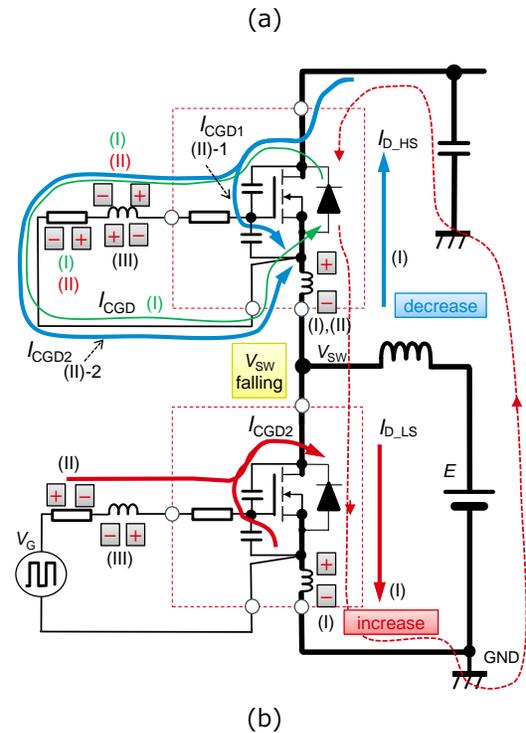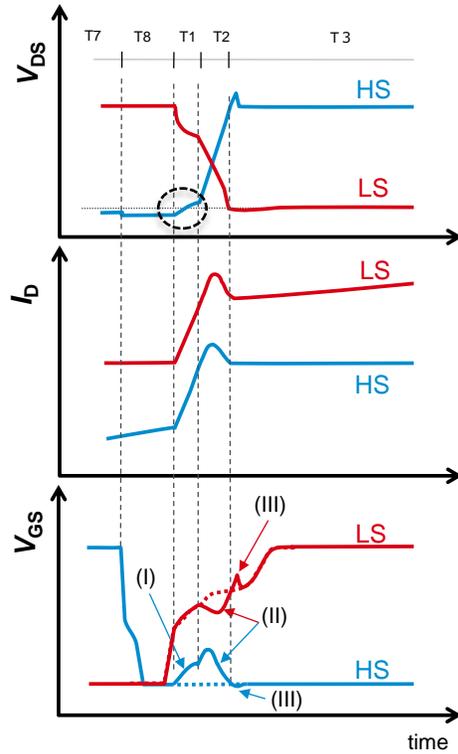

(b)

Figure 8. Behavior during turn on
(a) Waveforms, (b) Current flow on gate line

Figure 9 shows the V_{DS} waveforms on the switching side (LS) and commutation side (HS) at turn-on transient. It can be seen that V_{DS_HS} of the TO-247-4L rises rapidly just after switching transient starts.
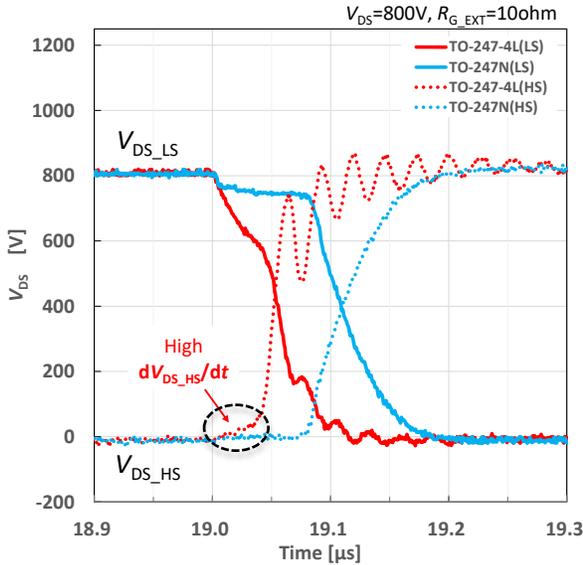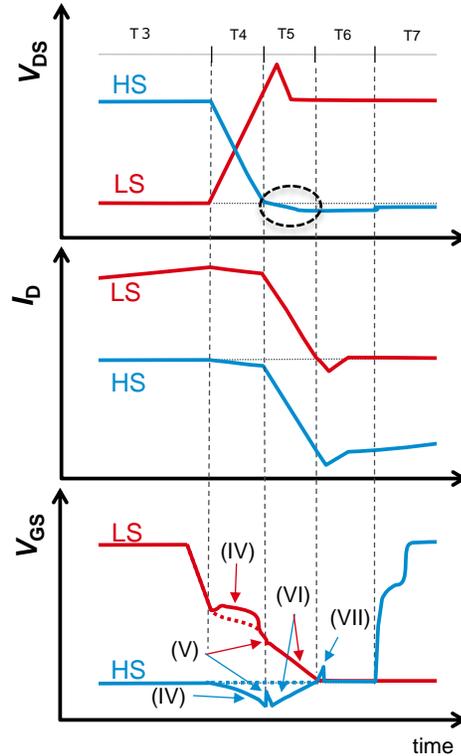

Figure 9. V_{DS} waveform during turn on

(a)

Switching behavior in Event (II) is also accelerated, and the current to charge C_{DS} flowing from HS to LS in Figure 8(b), also gets larger. According to such situation, for both as non-switching side as well as switching side may be necessary to take countermeasures to suppress surge voltage between drain and source.

The turn-off behavior with TO-247-4L is different from case of TO-247N for the event (VI) and event (VII), shown in Figure 9 (a).

Event (VI) has changes of I_D such as same behavior during turn on event (I). V_{F_HS} of the body diode rises sharply due to a rapid increase of I_{D_HS} on HS. Therefore, current I_{CGD} by dV_{F_HS}/dt flows again and leads to negative surge voltage. (Figure 10 (a) dashed circle)

Figure 11 shows the V_{DS} waveforms on the switching side (LS) and commutation side (HS) at turn-off transient. It can be seen that dV_{F_HS}/dt is generated as same situation with that during turn on. It happens because V_{DS} changes to negative side during I_D change (period T5) after HS V_{DS_HS} completes as theoretical trace of dV_{DS_HS}/dt (period T4).
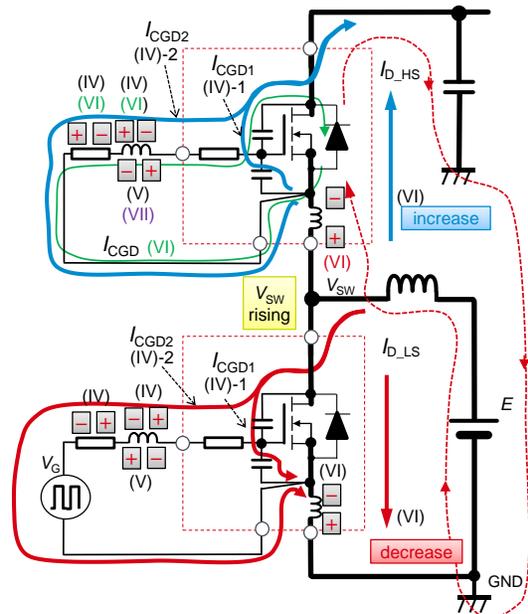
(b)

Figure 10. Behavior during turn on
(a) Waveforms, (b) Current flow on gate line

Regarding event (VII), after the period T5 is completed and I_{D_HS} does not change anymore, dV_{F_HS}/dt disappears, I_{CGD} does not flow into the gate terminal anymore. Therefore it may be observed positive surge voltage between gate and source, induced by the parasitic gate inductance L_{TRACE}. This positive surge in case of TO-247N hardly observes.
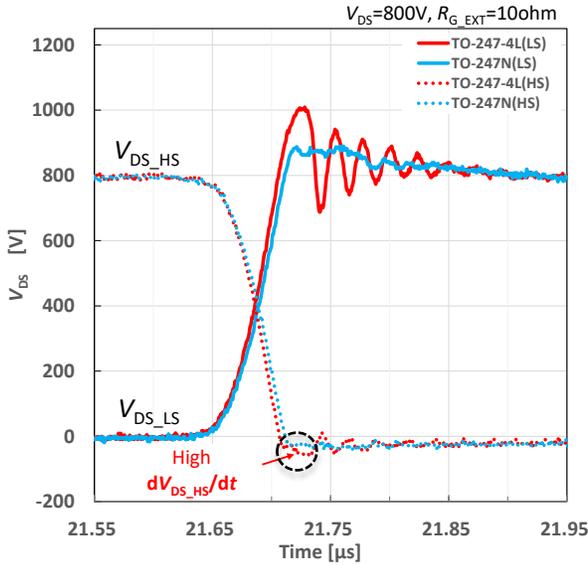

Figure 11. Waveform of V_{DS} during turn off

Figure 12 and Figure 13 show the V_{GS} waveform in the double pulse test using ROHM SCT3040KR, without countermeasures for surge voltage on gate path (Non-Protected), and with countermeasures to suppressed the gate surge voltages (Protected). In order to suppress these surges voltages, ROHM strongly recommends implementing a surge suppression circuit close to the MOSFET. For details, please refer to the application note "Surge suppression of gate-source voltage" (*2).
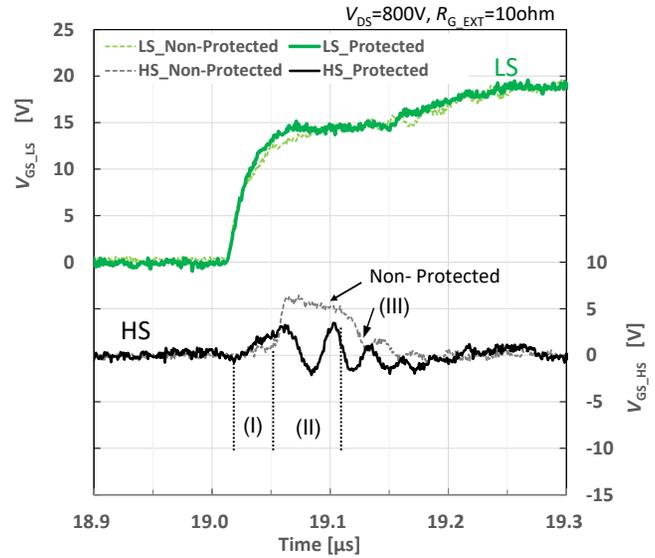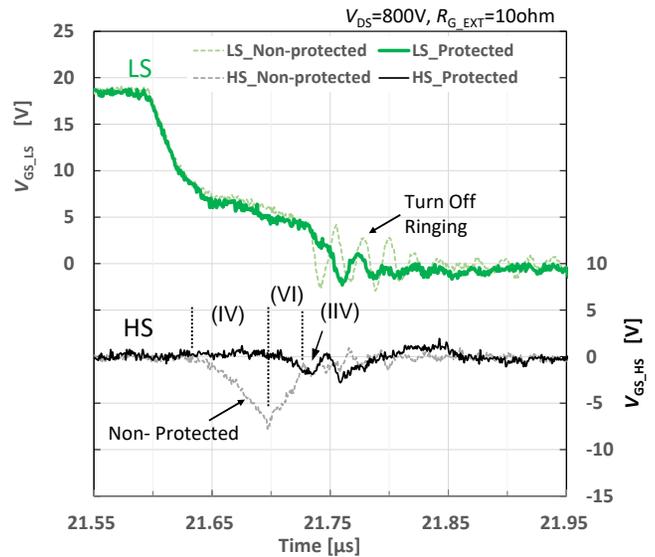

Figure 12. SCT3040KR V_{GS} during turn on

Figure 13. SCT3040KR V_{GS} during turn off

Notification for Layout

As final topics in this application note, we want to show notification related to layout with TO-247-4L.

As shown in Figure 3(a), gate terminal of TO-247-4L is on the right side toward the marking surface, but the TO-247N has gate terminal on the left side as shown in Figure 14. Driver ICs usually drives MOSFETs, but most of drivers ICs have pin assignments suitable for the conventional package as TO-247N.

Figure 15 shows connection diagrams for MOSFET and ROHM driver IC (BM61S40RFV-C).

In the case of (a) TO-247N, drive signal for MOSFET OUT and return signal (GND2) have the same arrangement as the Gate and Source terminals of device package, and the layout can be drawn in parallel on the same plane.

However, in case of (b) TO-247-4L, Gate and Driver Source terminal are opposite pin assignment for driver IC. It is not able to design the layout of gate and drive source path without crossing on same plane. Therefore, please pay attention to the area ratio of the loop areas (1) and (2) formed surrounded by the OUT signal and GND2 signal paths as shown in Figure 15(b).

This is because the dI_D / dt of TO-247-4L is quite high, and if the change in magnetic flux ($d\Phi / dt$) due to this current change is orthogonal to this loop area, induced voltage proportional to the loop area of drive circuit will be generated. Depending on ratio of loop area between gate and source of MOSFET, induced voltages may cause malfunction such as positive or negative surge voltages. For this reason, it is necessary to minimize loop area formed by OUT signal and GND2 signal as mentioned and make the loop (1) and the loop (2) equal.

We also recommend the installation of a V_{GS} surge suppression circuit, but V_{GS} surge may still exceed V_{GS} standard due to ringing V_{DS} during turn-off. In that case, reducing wiring impedance from HVdc or implementing surge countermeasure such as a snubber circuit for each MOSFET will help to suppress V_{GS} surge. For the snubber circuit design, please refer to the application note "Snubber circuit design method" (*3).
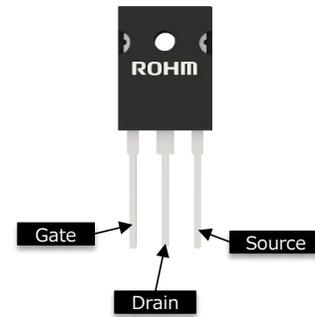

Figure 14. TO-247N pin assignment
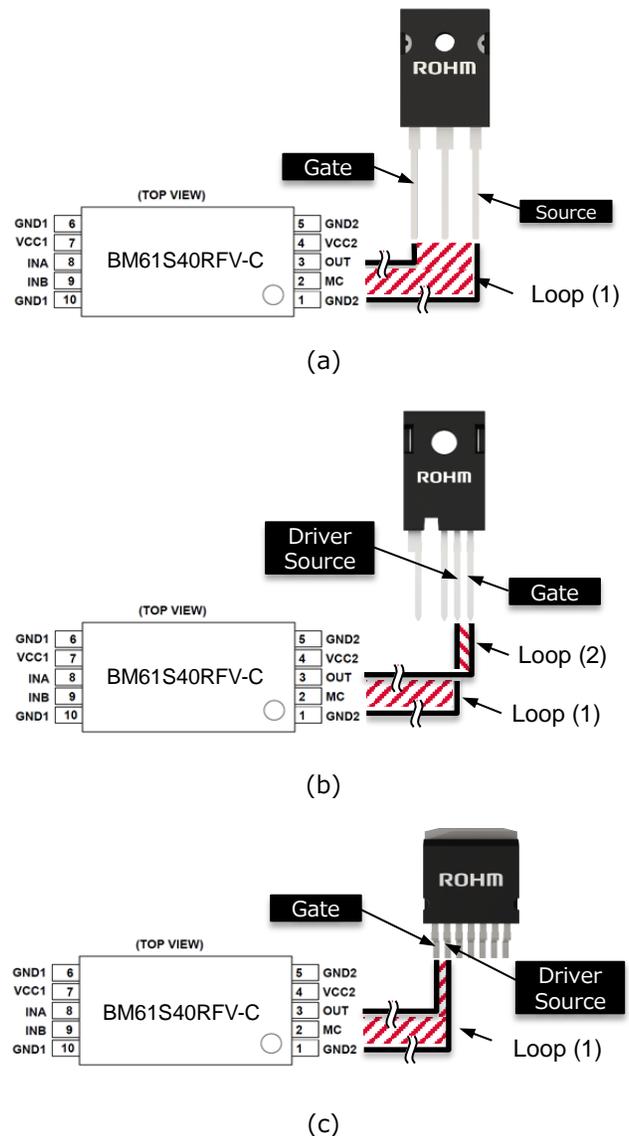

(a)

(b)

(c)

Figure 15. Examples of connection diagrams for MOSFET and ROHM driver IC (BM61S40RFV-C) (a) TO-247N, (b) TO-247-4L, (c) TO-263-7L

Summary

For MOSFETs with driver source terminal such as TO-247-4L and TO-263-7L, by taking care from early stage of circuit design about V_{GS} surge suppression and V_{DS} turn on ringing came from improvement of switching characteristics, it may be easier to take countermeasure for unexpected trouble in evaluation phase of your development process. We hope this application note can support you to handle properly high-speed package such as equipped with driver source terminal.

References :

*1 Gate-source voltage behaviour in a bridge configuration
  Application Note (No. 60AN135ERev.002)
  ROHM Co., Ltd.   April 2020

*2 Gate-source voltage surge suppression methods
  Application Note (No. 62AN010ERev.002)
  ROHM Co., Ltd.   April 2020

*3 Snubber circuit design methods
  Application Note (No. 62AN037ERev.002)
  ROHM Co., Ltd.   April 2020

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