

ROHM Solution Simulator

4.5V to 42V Input Voltage Range 3.5A Output Current Integrated FET BD9G401EFJ / Frequency Response

This circuit simulates the frequency response of BD9G401EFJ. You can observe the loop gain and measure phase margin. You can customize the simulation conditions by changing the parameters of components highlighted in blue. You can simulate the circuit in the published application note: Measurement Method for Phase Margin with FRA. [\[JP\]](#) [\[EN\]](#) [\[CN\]](#)

General Cautions

- Caution 1:** The values from the simulation results are not guaranteed. Use these results as a guide for your design.
- Caution 2:** These model characteristics are specifically at $T_a = 25\text{ }^\circ\text{C}$. Thus, the simulation result with temperature variances may significantly differ from the result with the one done at actual application board (actual measurement).
- Caution 3:** Please refer to the datasheet for details of the technical information.
- Caution 4:** The characteristics may change depending on the actual board design and ROHM strongly recommend to double check those characteristics with actual board where the chips will be mounted on.

1 Simulation Schematic

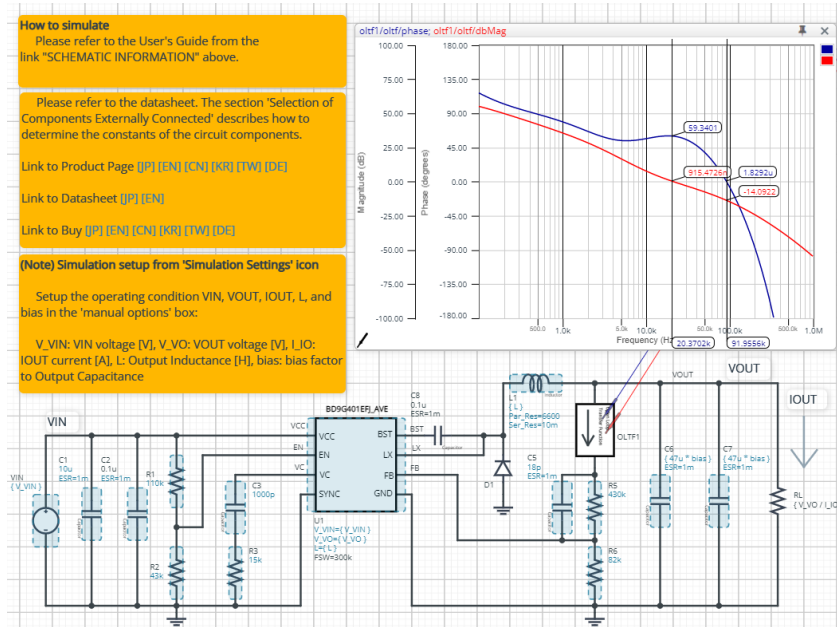


Figure 1. Simulation Circuit

2 How to simulate

The simulation settings, such as frequency range or convergence options, are configurable from the 'Simulation Settings' shown in Figure 2, and Table 1 shows the default setup of the simulation.

In case of simulation convergence issue, you can change advanced options to solve.

The parameters V_VIN , V_VO , I_IO , L and bias are defined in the 'Manual Options'.

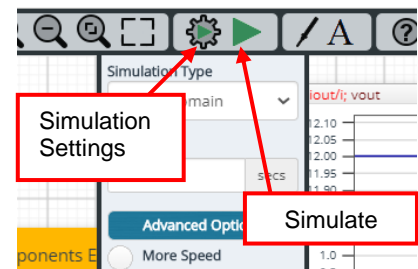


Figure 2. Simulation Settings and execution

Table 1. Simulation settings default setup

Parameters	Default	Note
Simulation Type	Frequency-Domain	(Do not change Simulation Type)
Start Frequency	100 Hz	Simulate the frequency response for the frequency range from 100 Hz to 1 MHz.
End Frequency	1Meg Hz	
Advanced options	Balanced Convergence Assist	
Manual Options	“.param V_VIN=12 V_VO=5 I_IO=3.5 L=22u bias=0.6”	See “Simulation Condition” for details

3 Simulation Conditions

3.1 How to define V_{IN} , V_{OUT} , I_{OUT} , L, and bias factor

These parameters are used to setup the simulation conditions and BD9G401EFJ_AVE model parameters, therefore these are defined in the Manual Options as the common variables.

Table 2 shows the default value of V_{IN} , V_{OUT} , I_{OUT} , L, and bias. Those values are defined and can be set in the 'Manual Options' text box from Simulation Settings as shown in Figure 3.

The input voltage V_{IN} , output inductance of L1, and the load resistance of RL are automatically set according to those parameters. Note that feedback resistors are not automatically set by V_{VO} . Set R1 and R2 manually.

Table 2. Simulation Conditions

Parameters	Variable Name	Default Value	Units	Descriptions
V_{IN}	V_VIN	12	V	Input Voltage
V_{OUT}	V_VO	5	V	Output Voltage
I_{OUT}	I_IO	3.5	A	Output Current
L	L	22u	H	Output Inductor
bias factor	bias	0.6	-	Bias factor to Output Capacitance

(Note 1) Set it to the guaranteed operating range of the DC/DC Converter.

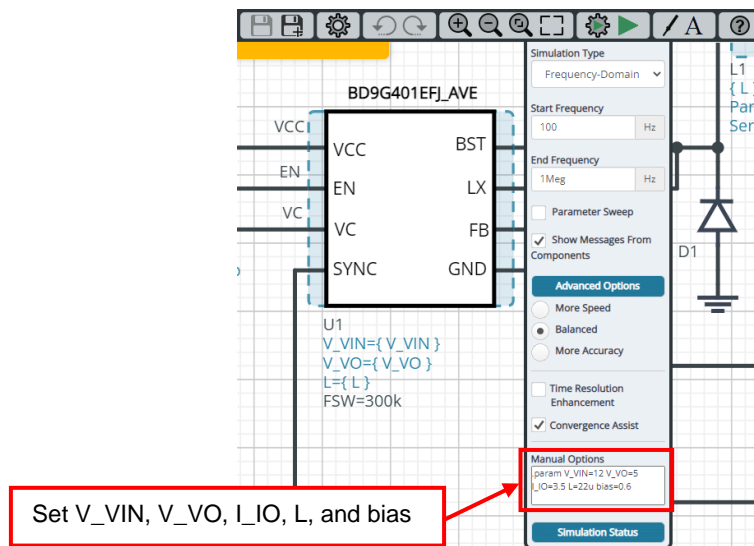


Figure 3. Definition of V_{IN} , V_{OUT} , I_{OUT} , L, and bias factor

3.2 Resistive Load RL

RL is the resistive load and its resistance is determined from V_{OUT} and I_{OUT} . The resistance value is defined by the equation below.

Table 3. Resistive load

Instance Name	Default Value	Unit
RL	$\{ V_{VO} / I_{IO} \}$	Ω

4 BD9G401EFJ_AVE model

The simulation model in this circuit is designed for frequency response, and the functions not related to frequency response are not implemented.

Table 4. BD9G401EFJ_AVE model pins used for frequency response

Pin Name	Description
VCC	Power supply input.
EN	Enable input.
VC	Error amplifier output terminal.
BST	Pin for bootstrap capacitor.
LX	Switching node.
FB	Output voltage feedback pin.
GND	Ground.

Table 5. BD9G401EFJ_AVE model pins NOT used for frequency response

Pin Name	Description
SYNC	Connected to ground (no external clock).

4.1 BD9G401EFJ_AVE Model Parameters

BD9G401EFJ_AVE model has its parameters shown in Table 6. All the parameters are pre-defined and fixed in the simulation. V_VIN is substituted to V_VIN as shown in Table 6.

Table 6. Parameter List

Parameters	Default Values	Description
V_VIN	V_VIN	VIN voltage
V_VO	V_VO	VOOUT voltage
L	L	Output inductance
FSW	300k	Switching Frequency

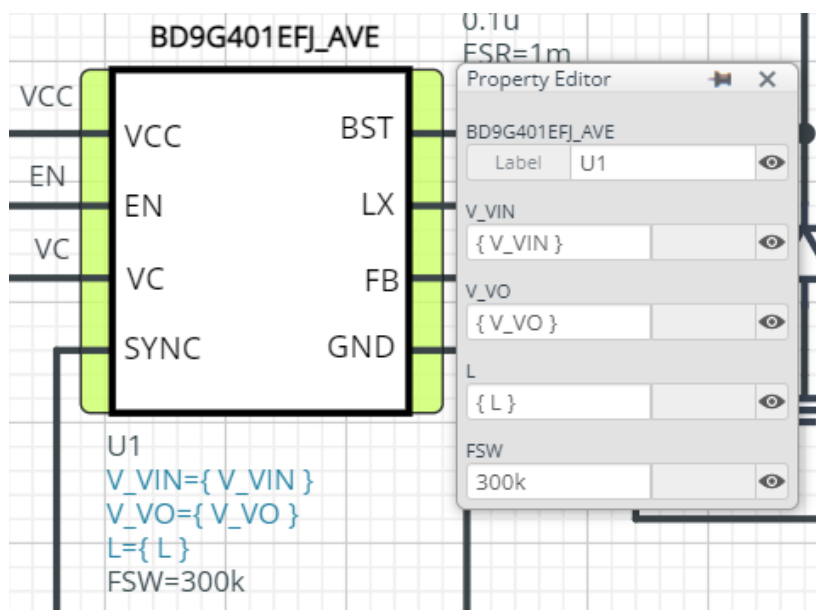


Figure 4. Property Editor of BD9G401EFJ_AVE model

5 Peripheral Components

To set parameters of components, open 'property' by double clicking or right clicking on a component. You can input a value to a property text box if available. Please refer to the hands-on manual for more details.

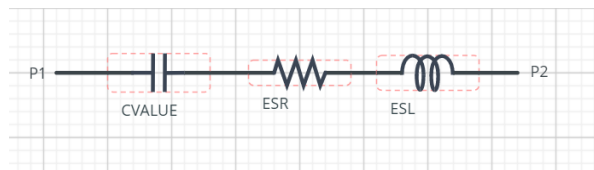
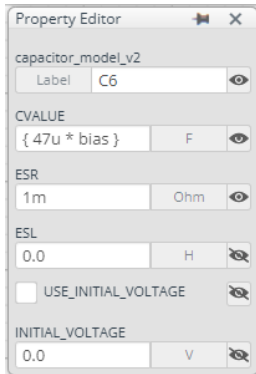
5.1 Bill of Material

Table 7 shows the list of components used in the simulation schematic. Each of the capacitor and inductor has the parameters of equivalent circuit shown below. The default value of equivalent components are set to zero except for the parallel resistance of L and series resistance of capacitors. You can modify the values of each component.

Table 7. List of components used in the simulation circuit

Type	Instance Name	Default Value	Units
Capacitor	C1	10	μF
	C2	0.1	μF
	C3	1000	pF
	C5	18	pF
	C6	47	μF
	C7	47	μF
	C8	0.1	μF
Inductor	L1	22	μH
Resistor	R1	110	$\text{k}\Omega$
	R2	43	$\text{k}\Omega$
	R3	15	$\text{k}\Omega$
	R5	430	$\text{k}\Omega$
	R6	82	$\text{k}\Omega$

5.2 Capacitor Equivalent Circuits



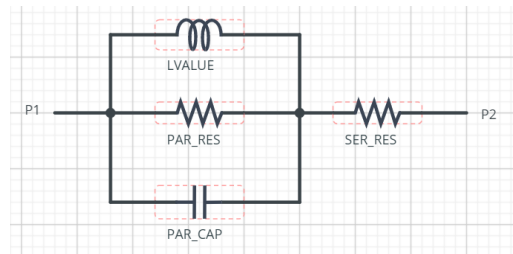
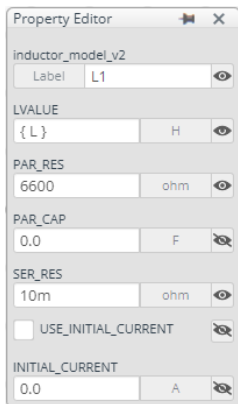
(a) Property editor

(b) Equivalent circuit

Figure 5. Capacitor property editor and equivalent circuit

The default value of ESR is 1 m Ω .

5.3 Inductor Equivalent Circuits



(a) Property editor

(b) Equivalent circuit

Figure 6. Inductor property editor and equivalent circuit

The default value of PAR_RES is 6.6 k Ω .

(Note 2) These parameters can take any positive value or zero in simulation but it does not guarantee the operation of the IC in any condition. Refer to the datasheet to determine adequate value of parameters.

6 Open Loop Transfer Function (OLTF) Monitor

OLTF is the insert model to measure AC open loop transfer function and is inserted to acquire the gain and phase output. To monitor the gain and phase from OLTF, select probe items 'dbMag' for gain and 'phase' for phase plot, respectively from 'property' of OLTF.

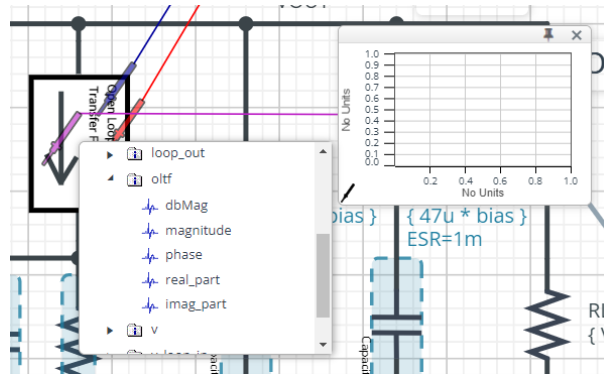


Figure 7. Probe Items of OLTF

7 Link to the product information and tools

7.1 DC/DC Converter

BD9G401EFJ-M : Integrated FET 1ch Buck Converter. [\[JP\]](#) [\[EN\]](#) [\[CN\]](#) [\[KR\]](#) [\[TW\]](#) [\[DE\]](#)

BD9G401UEFJ-M : Integrated FET 1ch Buck Converter. [\[JP\]](#) [\[EN\]](#) [\[CN\]](#) [\[KR\]](#) [\[TW\]](#) [\[DE\]](#)

7.2 General Purpose Chip Resistors

MCR01MZPF : Thick Film Chip Resistors. [\[JP\]](#) [\[EN\]](#) [\[CN\]](#) [\[KR\]](#) [\[TW\]](#) [\[DE\]](#)

7.3 Schottky Barrier Diode for general rectification

RBR3LAM60BTF : Schottky Barrier Diode. [\[JP\]](#) [\[EN\]](#) [\[CN\]](#) [\[KR\]](#) [\[TW\]](#) [\[DE\]](#)

RBR3LAM60B : Schottky Barrier Diode. [\[JP\]](#) [\[EN\]](#) [\[CN\]](#) [\[KR\]](#) [\[TW\]](#) [\[DE\]](#)

Technical Articles and Tools can be found in the Design Resources on the product web page.

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