ROHM Solution Simulator

4.5 V to 36 V Input, 5 A Integrated MOSFET Single Synchronous Buck DC/DC Converter

BD9F500QUZ / Frequency Response

This circuit simulates the frequency response of BD9F500QUZ. You can observe the loop gain and measure phase margin. You can customize the simulation conditions by changing the parameters of components highlighted in blue.

You can simulate the circuit in the published application note: Measurement Method for Phase Margin w/ FRA. [JP] [EN] [CN]

General Cautions

Caution 1: The values from the simulation results are not guaranteed. Use these results as a guide for your design.

Caution 2: These model characteristics are specifically at Ta = 25 °C. Thus, the simulation result with temperature variances may significantly differ from the result with the one done at actual application board (actual measurement).

Caution 3: Please refer to the datasheet for details of the technical information.

Caution 4: The characteristics may change depending on the actual board design and ROHM strongly recommend to double check those characteristics with actual board where the chips will be mounted on.

1 Simulation Schematic

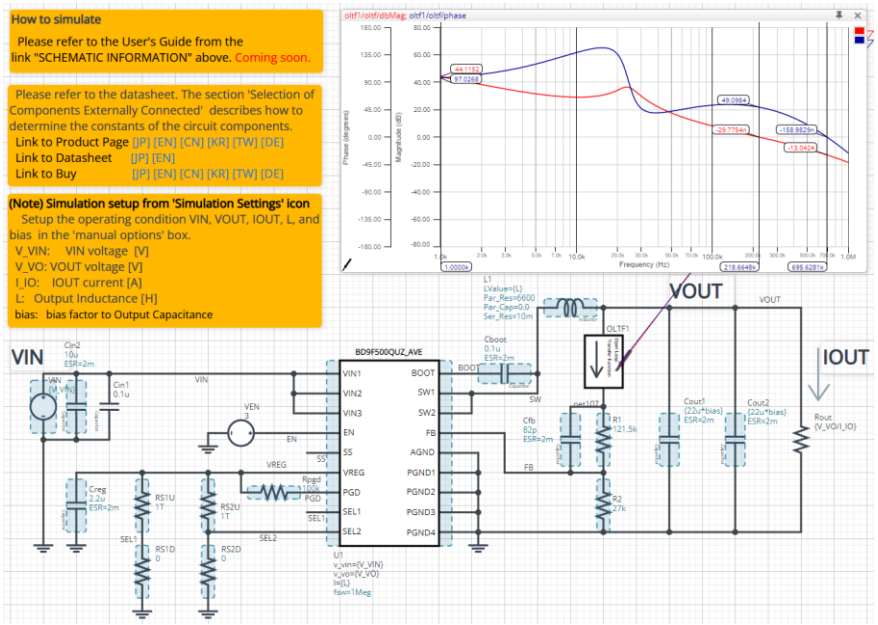


Figure 1. Simulation Circuit

2 How to simulate

The simulation settings, such as frequency range or convergence options, are configurable from the 'Simulation Settings' shown in Figure 2, and Table 1 shows the default setup of the simulation.

In case of simulation convergence issue, you can change advanced options to solve.

The parameters V_VIN, V_VO, I_IO, L and bias are defined in the 'Manual Options'.

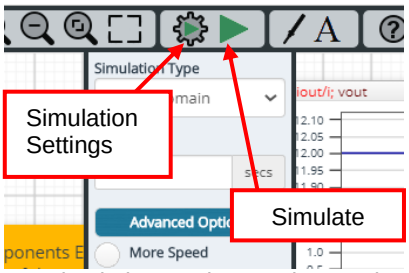


Figure 2. Simulation Settings and execution

Table 1. Simulation settings default setup

Parameters	Default	Note
Simulation Type	Frequency-Domain	(Do not change Simulation Type)
Start Frequency	1k Hz	Simulate the frequency response for the frequency range from 1 kHz to 1 MHz.
End Frequency	1Meg Hz	
Advanced options	Balanced Convergence Assist	
Manual Options	".param V_VIN=12 V_VO=3.3 I_IO=3 L=1.5u bias=0.69"	*See "Simulation Condition" for details*

3 Simulation Conditions

3.1 How to define V_{IN}, V_{OUT}, I_{OUT}, L, and bias factor

These parameters are used to setup the simulation conditions and BD9F500QUZ_AVE model parameters, therefore these are defined in the Manual Options as the common variables.

Table 2 shows the default value of V_{IN}, V_{OUT}, I_{OUT}, L, and bias. Those values are defined and can be set in the 'Manual Options' text box from Simulation Settings as shown in Figure 3.

The output voltage of VIN, output inductance of L1, and the load resistance of Rout are automatically set according to those parameters. Note that feedback resistors are not automatically set by V_VO. Set R1 and R2 manually.

Table 2. Simulation Conditions

Parameters	Variable Name	Default Value	Units	Descriptions
V_{IN}	V_VIN	12	V	Input Voltage
V_{OUT}	V_VO	3.3	V	Output Voltage
I_{OUT}	I_IO	3	A	Output Current
L	L	1.5u	H	Output Inductor
bias factor	bias	0.69	-	Bias factor to Output Capacitance

(Note 1) Set it to the guaranteed operating range of the DC/DC Converter.

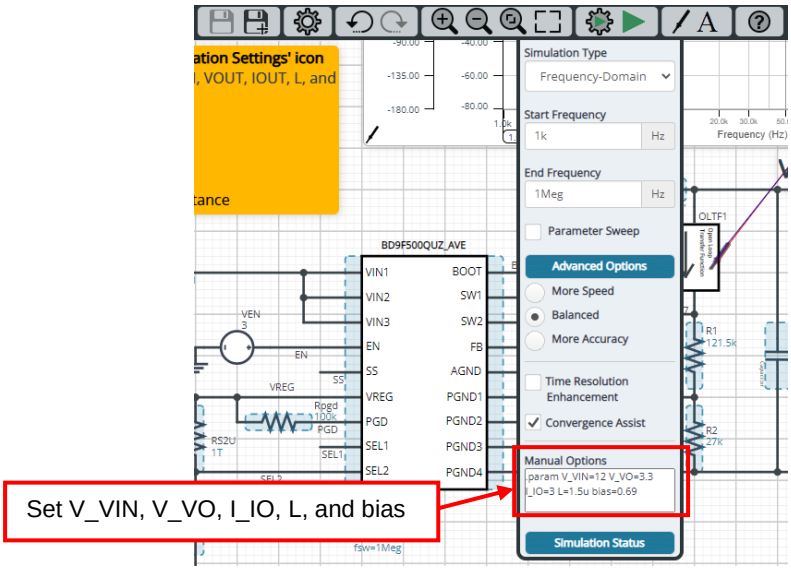


Figure 3. Definition of V_{IN}, V_{OUT}, I_{OUT}, L, and bias factor

3.2 Resistive Load Rout

Rout is the resistive load and its resistance is determined from V_{OUT} and I_{OUT}. The resistance value is defined as the equation below.

Table 3. Resistive load

Instance Name	Default Value	Unit
Rout	{V_VO/I_IO}	Ω

3.3 Setting Switching Control Mode

SEL1 and SEL2 pin conditions can be either GND, OPEN, or VREG. To implement these, R_{SXU} pull-up resistor to VREG and R_{SXD} pull-down resistor to GND is used. These resistors' value can have either 0 Ω or 1 TΩ. 0 Ω is used for Short; 1 TΩ is used for - or Open in the Recommended Component Values in the datasheet's Application Examples.

Table 4. SEL1 and SEL2 Pin Conditions with varying RSXU, RSXD

RSXU	RSXD	Outcome
0	0	Invalid: VREG is shorted to GND
0	1T	SELX = VREG
1T	0	SELX = GND
1T	1T	SELX = OPEN

(Note 2) Set it to the guaranteed operating condition of the DC/DC Converter.

4 BD9F500QUZ_AVE model

The simulation model in this circuit is designed for frequency response, and the functions not related to frequency response are not implemented.

Table 5. BD9F500QUZ_AVE model pins used for frequency response

Pin Name	Description
VIN	Power supply input.
EN	Enable input.
VREG	Internal power supply output pin.
SEL1, SEL2	Pins for setting switching control mode.
BOOT	Pin for bootstrap.
SW	Switching node.
FB	Output voltage feedback pin. Inverting input node of the error amplifier.
AGND, PGND	Ground.

Table 6. BD9F500QUZ_AVE model pins NOT used for frequency response

Pin Name	Description
SS	Input is ignored (no switching operation in this model).
PGD	Output is ignored (no power good in this model).

4.1 BD9F500QUZ_AVE Model Parameters

BD9F500QUZ_AVE model has its parameters shown in Table 7. All the parameters are pre-defined and fixed in the simulation. V_VIN is substituted to V_VIN as shown in Table 7. FSW allowed values are 600k, 1Meg, 2.2Meg.

Table 7. Parameter List

Parameters	Default Values	Description
V_VIN	V_VIN	VIN voltage
V_VO	V_VO	VOUT voltage
L	L	Output inductance
FSW	1Meg	Switching Frequency

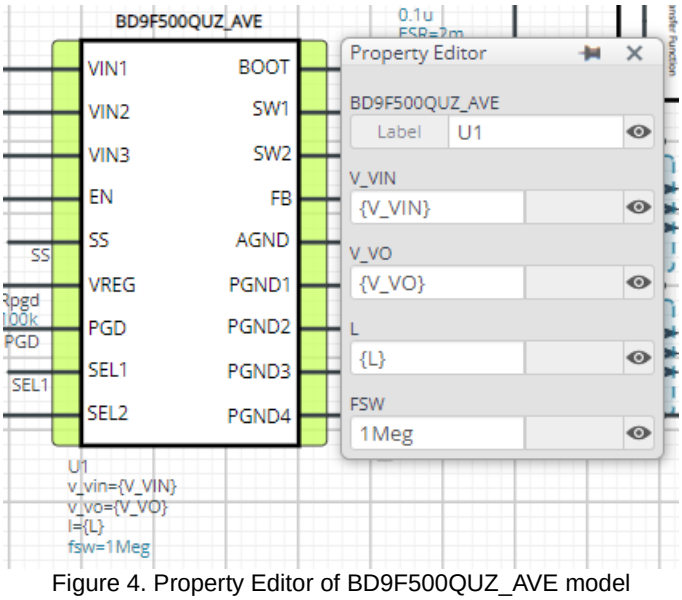


Figure 4. Property Editor of BD9F500QUZ_AVE model

5 Peripheral Components

To set parameters of components, open 'property' by double click or right click on a component. You can input a value to a property text box if available. Please refer to the hands-on manual for more details.

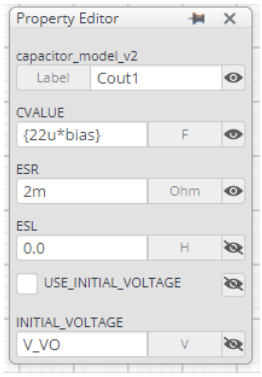
5.1 Bill of Material

Table 8 shows the list of components used in the simulation schematic. Each of the capacitor and inductor has the parameters of equivalent circuit shown below. The default value of equivalent components are set to zero except for the parallel resistance of L and series resistance of capacitors. You can modify the values of each component.

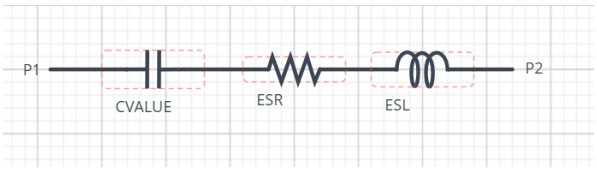
Table 8. List of components used in the simulation circuit

Type	Instance Name	Default Value	Units
Capacitor	Cin1	0.1	µF
	Cin2	10	µF
	Cboot	0.1	µF
	Cout1	22	µF
	Cout2	22	µF
	Creg	2.2	µF
	Cfb	82	pF
Inductor	L1	1.5	µH
Resistor	R1	121.5	kΩ
	R2	27	kΩ
	Rpgd	100	kΩ

5.2 Capacitor Equivalent Circuits



(a) Property editor

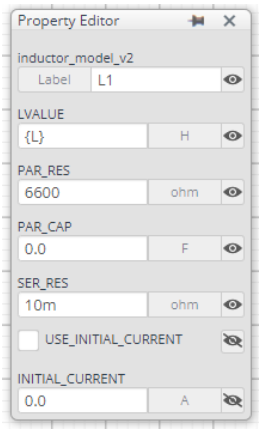


(b) Equivalent circuit

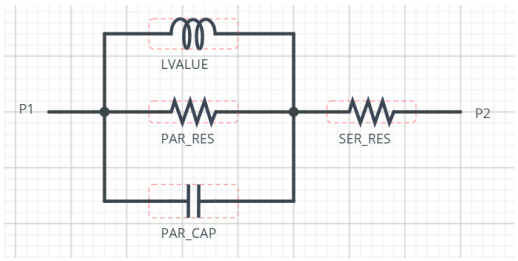
Figure 5. Capacitor property editor and equivalent circuit

The default value of ESR is 2 mΩ.

5.3 Inductor Equivalent Circuits



(a) Property editor



(b) Equivalent circuit

Figure 6. Inductor property editor and equivalent circuit

The default value of PAR_RES is 6.6 kΩ.

(Note 3) These parameters can take any positive value or zero in simulation but it does not guarantee the operation of the IC in any condition. Refer to the datasheet to determine adequate value of parameters.

6 Open Loop Transfer Function (OLTF) Monitor

OLTF1 is the insert model to measure AC open loop transfer function and is inserted to acquire the gain and phase output. To monitor the gain and phase from OLTF1, select probe items 'dbMag' for gain and 'phase' for phase plot, respectively from 'property' of OLTF1.

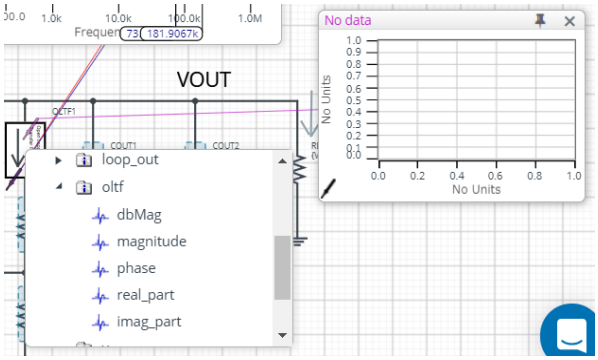


Figure 7. Probe Items of OLTF1

7 Link to the product information and tools

7.1 DC/DC Converter

BD9F500QUZ : Integrated MOSFET Single Synchronous Buck DC/DC Converter. [JP] [EN] [CN] [KR] [TW] [DE]

7.2 General Purpose Chip Resistors

MCR01MZPF : Thick Film Chip Resistors. [JP] [EN] [CN] [KR] [TW] [DE]

Technical Articles and Tools can be found in the Design Resources on the product web page.